LISTING OF CLAIMS

1. (previously presented) A method for singulating semiconductor components contained on a substrate having a plurality of locator openings comprising:

providing a nest, a base configured to hold the nest, and a plurality of locator pins on the base configured to engage the locator openings;

placing the nest on the base wherein the base comprises a plurality of mounting studs configured to engage a plurality of mounting openings on the nest;

placing the substrate on the nest and aligning the substrate using the locator pins;

removing the nest from the base; and

sawing the substrate on the nest into separate components.

2. (previously presented) The method of claim 1 further comprising providing a clamping mechanism attachable to the nest and holding the substrate on the nest prior to the removing step using the clamping mechanism.

Claim 3 (canceled)

4. (previously presented) The method of claim 1 wherein the locator pins project through openings in the nest.

5. (original) The method of claim 1 wherein the components comprise an element selected from the group consisting of packages, multi chip modules, printed circuit boards, interconnects, bumped dice and bare dice.

6. (original) The method of claim 1 wherein the substrate comprises a panel and the components are arranged on the panel in at least one row.

7. (original) The method of claim 1 wherein the substrate comprises a panel and the components are arranged on the panel in a matrix of rows and columns.

8. (previously presented) The method of claim 1 further comprising providing a sawing base configured to hold the nest and holding the nest on the sawing base during the sawing step.

9. (previously presented) A method for singulating semiconductor components contained on a substrate having a plurality of locator openings comprising:

providing a nest configured to hold the substrate;

providing an alignment base comprising a plurality of locator pins configured to engage the locator openings;

placing the substrate on the nest;

placing the nest on the alignment base and aligning the substrate on the nest using the locator pins wherein the alignment base comprises a plurality of mounting studs configured to engage a plurality of mounting openings on the nest;

providing a sawing base configured to hold the nest and the substrate for sawing;

removing the nest from the alignment base;

placing the nest on the sawing base; and

sawing the substrate into separate components.

10. (original) The method of claim 9 wherein the sawing base comprises a vacuum opening configured to hold the substrate during the sawing step.

11. (previously presented) The method of claim 9 wherein the nest comprises a detachable clamping mechanism and further comprising detaching the clamping mechanism prior to the sawing step.

12. (original) The method of claim 9 wherein the nest comprises a detachable clamping mechanism and at least some of the locator pins are mounted to the clamping mechanism.

13. (original) The method of claim 9 further comprising clamping the substrate to the nest following the placing the nest step, then unclamping the substrate from the nest prior to the sawing step.

14. (previously presented) A method for singulating semiconductor components contained on a substrate having a plurality of locator openings comprising:

providing an alignment base comprising a plurality of locator pins configured to engage the locator openings;

providing a nest mountable to the alignment base configured to hold the substrate;

placing the nest on the alignment base wherein the alignment base comprises a plurality of mounting studs configured to engage a plurality of mounting openings on the nest;

aligning the substrate on the nest using the alignment base and the locator pins;

providing a sawing base for holding the nest comprising a vacuum opening configured to hold the substrate on the nest;

removing the nest from the alignment base;

mounting the nest to the sawing base with the vacuum opening holding the substrate on the nest; and

sawing the substrate into separate components.

15. (original) The method of claim 14 wherein the substrate comprises a panel, and the components are arranged on the panel in at least one row.

16. (original) The method of claim 14 wherein the substrate comprises a panel, and the components are arranged on the panel in one or more matrix arrays of rows and columns.

17. (original) The method of claim 14 further comprising providing a clamping mechanism configured for attachment to the nest for holding the substrate on the nest, attaching the clamping mechanism to the nest following the aligning step, then removing the clamping mechanism from the nest prior to the sawing step.

18. (original) The method of claim 17 further comprising providing the clamping mechanism with at least some of the locator pins.

19. (previously presented) A method for singulating semiconductor components contained on a substrate:

providing the substrate with a plurality of locator openings;

providing a nest configured to hold the substrate comprising a plurality of openings;

providing a clamping mechanism attachable to the nest for clamping the substrate to the nest;

providing an alignment base comprising a plurality of locator pins configured to engage the locator openings;

placing the nest on the alignment base with the locator pins projecting from the openings in the nest;

placing the substrate on the nest with the locator pins engaging the locator openings;

attaching the clamping mechanism to the nest to clamp the substrate to the nest;

removing the nest from the alignment base;

providing a sawing base comprising a vacuum opening configured to apply a vacuum to the substrate held on the nest;

applying the vacuum through the sawing base to the substrate;

removing the clamping mechanism from the nest; and

sawing the substrate held on the nest by the vacuum into separate components.

20. (original) The method of claim 19 further comprising providing the clamping mechanism with a plurality of second locator pins configured to engage the locator openings.

21. (original) The method of claim 19 further comprising providing a saw blade configured to perform the sawing step.

22. (original) The method of claim 19 wherein the clamping mechanism comprises latches for engaging the nest, and a compliant pad configured to engage the components.

23. (original) The method of claim 19 wherein the nest comprises a plurality of recesses configured to retain the components on the substrate.

24. (original) The method of claim 19 wherein the alignment base comprises a plurality of first mounting studs configured to engage a plurality mounting openings on the nest.

25. (original) The method of claim 19 wherein the sawing base comprises a plurality of second mounting studs configured to engage the mounting openings on the nest.

26-55 (canceled)

56. (currently amended) A method for singulating semiconductor components contained on a substrate having a plurality of locator openings comprising:

providing a base comprising a plurality of mounting studs and a nest configured to hold the substrate comprising a plurality of mounting openings;

providing a clamping mechanism configured to hold the component on the base and a plurality of locator pins on the clamping mechanism configured to engage the locator openings ~~wherein the base comprises a plurality of mounting studs configured to engage a plurality of mounting openings on the nest~~;

placing the nest on the base and the substrate on the nest with the mounting studs engaging the mounting openings;

attaching the clamping mechanism to the nest;

aligning the substrate on the nest during the attaching step using the locator pins;

providing a sawing base configured to hold the nest and the substrate for sawing;

removing the nest from the base;

placing the nest on the sawing base; and

sawing the substrate into separate components.

REMARKS

This Amendment incorporates the limitations to claims 1, 9 and 14 from the Examiner's Amendment in the Notice Of Allowance dated 09/30/2003. However, the limitations added to claim 56 at line 11, have been deleted and incorporated at lines 4-6 and 14 of claim 56. These amendments are required to make claim 56 more definite.

Should any issues remain, the Examiner is asked to contact the undersigned by telephone.

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October 6, 2003
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Stephen A. Gratton, Attorney for Applicants